

sub
F1

14. A system according to Claim 13, wherein the threshold condition is a function of the difference between the local clock value and the program clock value.

By

15. A system according to Claim 13, wherein said hardware includes

means for monitoring for the occurrences of the threshold condition; and

means for transmitting a signal to the processor when the threshold condition occurs.--

REMARKS

In the Office Action, the Examiner rejected Claims 1, 2, 6, 11 and 12 under 35 U.S.C. §102(b) as being fully anticipated by a paper "RFC 1305 Network Time Protocol (Version 3)," (Mills). The Examiner objected to Claims 3-5 and 7-10 as being dependent upon rejected base claims, and the Examiner indicated that these claims would be allowable if rewritten in independent form including all of the limitations of the respective base claims and any intervening claims.

In response to the Office Action, Claims 3 and 7 are herein being rewritten in independent form. Also, this opportunity is being taken to amend Claim 1 to better distinguish over the prior art, and to add new Claims 13-15 to define the invention in an alternative manner. Claims 6, 11 and 12 are being cancelled to reduce the number of pending claims.

More specifically, Claim 3 is being rewritten in independent form including all of the limitations of Claims 1 and 2, and Claim 7 is being rewritten in independent form including

all of the limitations of Claim 6. Applicant respectfully submits that this places Claims 6 and 7, as well as Claims 4 and 5, which are dependent on Claim 3, and Claims 8-10, which are all dependent on Claim 7, in condition for allowance without any further argument or discussion. Accordingly, the Examiner is respectfully requested to reconsider and to withdraw the objection to Claims 3-5 and 7-10, and to allow these claims.

Claim 1 has been amended to include the limitations that hardware is used to adjust the local clock frequency until a threshold condition occurs, and after that, the processor is used to adjust that local clock frequency. As the Examiner has recognized, the use of hardware and software, in this combination, to adjust the local clock frequency is not disclosed or suggested by the prior art. This approach has a number of advantages. For instance, the software can be used to reduce the difference between the local and program clock frequencies when that difference is relatively large, and then after that difference has been reduced to a certain point, the faster hardware can be used to exactly match the local and program clock frequencies.

Because of the above-discussed differences between Claim 1 and the prior art, and because of the advantages associated with those differences, Claim 1 patentably distinguishes over the prior art and is allowable. The Examiner is, accordingly, requested to reconsider and to withdraw the rejection of Claim 1, and Claim 2, which is dependent on Claim 1, and to allow claims 1 and 2.

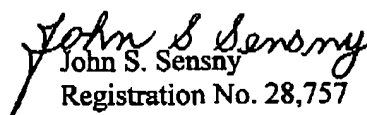
New Independent Claim 13 is directed to a system for adjusting a local clock, and includes limitations analogous to those discussed above in connection with Claim 1. In particular, Claim 13 positively sets forth the elements of hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and processor also on

the decoder and having a software program for adjusting the local clock frequency after that threshold condition occurs. For reasons analogous to those advanced above, the prior art also does not disclose or render obvious the subject matter of new Claim 13. Thus, Claim 13 and new Claims 14 and 15, which are dependent on Claim 13, are allowable.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

For the reasons set forth above, the Examiner is requested to reconsider and to withdraw the rejection of Claims 1 and 2 and the objection to Claims 3-5 and 7-10, and to allow Claims 1-5, 7-10 and 13-15. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is requested to telephone the undersigned.

Respectfully submitted,


John S. Sensny
Registration No. 28,757

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Garden City, New York 11530

JSS:gc

Serial No: 09/052,673

Docket: END919980042US1(11232)

VERSION WITH MARKINGS TO SHOW CHANGES MADE**IN THE CLAIMS**

Cancel Claims 11 and 12.

Amend Claims 1, 3 and 7, and add new Claims 13-15 as set forth below.

1. (Twice Amended) A method of adjusting a local clock of a digital data decoder, wherein the decoder includes hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, the method [frequency,] comprising the steps of :

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;
including the steps of:

i) using the hardware to adjust the local clock frequency until a threshold condition occurs,
and

iii) after the threshold condition occurs, using the processor to adjust the local clock frequency.

3. (Once Amended) [A method according to Claim 2,] A method of adjusting a local clock of a digital data decoder, wherein the clock oscillates at a local clock frequency, the method further comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

maintaining a local clock value based on the oscillations of the local clock;

receiving clock time stamps at the decoder which specify the program clock value and frequency;

maintaining a program clock value based on the clock signals received at the decoder;

determining if there is any difference between the local clock and the program clock frequencies;

determining if there is an absolute difference between the local clock value and the program clock value;

if there is either a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and

wherein the decoder includes hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, and wherein the step of adjusting the frequency of the local clock includes the steps of:

using the hardware to adjust the local clock frequency until a threshold condition occurs; and

after the threshold condition occurs, using the processor to adjust the local clock frequency.

7. (Once Amended) A system [according to Claim 6,] for adjusting a local clock on a digital data decoder, wherein the clock oscillates at a local clock frequency, the system comprising:

means for maintaining a local clock value based on the oscillations of the local clock;

means for receiving clock signals transmitted to the decoder at a program clock frequency;

means for maintaining a program clock value based on the clock signals transmitted to the decoder;

means for determining if there is any difference between the local clock and the program clock frequencies;

means for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and the program clock value, so that said difference approaches zero;

wherein the means for adjusting the frequency at which the local clock oscillates includes:

hardware for adjusting the local clock frequency until a threshold condition occurs; and

a processor having a software program for adjusting the local clock frequency after the threshold condition occurs.

--13. A system for adjusting a local clock of a digital data decoder, comprising:

means for determining if there is any difference between the local and program clock frequencies;

means for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock values, or an absolute difference

between the local clock value and the program value, so that said difference approaches zero, wherein the means for adjusting includes

i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.

14. A system according to Claim 13, wherein the threshold condition is a function of the difference between the local clock value and the program clock value.

15. A system according to Claim 13, wherein said hardware includes

means for monitoring for the occurrences of the threshold condition; and

means for transmitting a signal to the processor when the threshold condition occurs.--